

What is Claimed:

- 1 1. A multi chip module substrate comprising:
2 a plurality of chip sites each having:
3 (a) a plurality of signal vias, and
4 (b) a plurality of repair vias;
5 a circuit line net having a plurality of circuit lines, each said circuit line
6 extending between and intended to electrically connect selected signal vias; and
7 a repair line net having a plurality of groups of repair lines, each said
8 repair line extending between and electrically connecting a repair via of one said chip site
9 and a repair via of another said chip site.
- 1 2. A multi chip module substrate according to claim 1 wherein said
2 circuit lines are within said chip sites and said repair lines are within said chip sites.
- 1 3. A multi chip module substrate according to claim 1 wherein said
2 repair vias are outside of and surrounding an array of said signal vias.
- 1 4. A multi chip module substrate according to claim 3 wherein said
2 chip sites are identical.
- 1 5. A multi chip module substrate according to claim 1 wherein said
2 repair vias are disposed uniformly outside of and surrounding an array of said signal vias.
- 1 6. A multi chip module substrate according to claim 5 wherein said
2 chip sites are identical.

- 1 7. A multi chip module substrate according to claim 1 further
2 including:
- 3 (a) a first jumper connection extending between and
4 electrically connecting a first signal via in a first chip site
5 and that repair via in said first chip site that is connected to
6 a repair via in a second chip site in which a second signal
7 via is located and to which said first signal via is intended
8 to be connected; and
- 9 (b) a second jumper connection extending between and
10 electrically connecting said second signal via in said second
11 chip site and that repair via in said second chip site that is
12 connected to said repair via in said first chip site to which
13 said first signal via is electrically connected.
- 1 8. A multi chip module substrate according to claim 7 wherein said
2 circuit lines are within said chip sites and said repair lines are within said chip sites.
- 1 9. A multi chip module substrate according to claim 7 wherein said
2 repair vias are outside of and surrounding an array of said signal vias.
- 1 10. A multi chip module substrate according to claim 9 wherein said
2 chip sites are identical.
- 1 11. A multi chip module substrate according to claim 7 wherein said
2 repair vias are disposed uniformly outside of and surrounding an array of said signal vias.
- 1 12. A multi chip module substrate according to claim 11 wherein said
2 chip sites are identical.

1 13. A multi chip module substrate according to claim 1 wherein:
2 (a) the number of said repair vias in each said chip site is equal
3 to the number of said chip sites minus one,
4 (b) the number of said groups of said repair lines is equal to the
5 number of said chip sites, and
6 (c) the number of said repair lines in each said group is equal
7 to the number of said chip sites minus one.

1 14. A multi chip module substrate according to claim 4 wherein:
2 (a) the number of said repair vias in each said chip site is equal
3 to the number of said chip sites minus one,
4 (b) the number of said groups of said repair lines is equal to the
5 number of said chip sites, and
6 (c) the number of said repair lines in each said group is equal
7 to the number of said chip sites minus one.

1 15. A multi chip module substrate according to claim 7 wherein:
2 (a) the number of said repair vias in each said chip site is equal
3 to the number of said chip sites minus one,
4 (b) the number of said groups of said repair lines is equal to the
5 number of said chip sites, and
6 (c) the number of said repair lines in each said group is equal
7 to the number of said chip sites minus one.

1 16. A method of repairing an electronic package comprising the steps
2 of:

3 providing a multi chip module substrate including:

4 (a) a plurality of chip sites each having:

5 (1) plurality of signal vias, and

6 (2) plurality of repair vias,

7 (b) a circuit line net having a plurality of circuit lines, each said
8 circuit line extending between and intended to electrically
9 connect selected signal vias, and

10 (c) a repair line net having a plurality of groups of repair lines,
11 each said repair line extending between and electrically
12 connecting a repair via of one said chip site and a repair via
13 of another said chip site;

14 identifying in a circuit intended to be composed of:

15 (a) a first signal via in a first chip site,

16 (b) a second signal via in a second chip site, and

17 (c) a circuit line extending between and intended to electrically
18 connect said first signal via and said second signal via

19 a defect in one of:

20 (a) said first signal via,

21 (b) said second signal via, and

22 (c) said circuit line extending between and intended to
23 electrically connect said first signal via and said second
24 signal via;

25 isolating said first signal via;

26 isolating said second signal via;

27 electrically connecting said first signal via in said first chip site to that
28 repair via in said first chip site that is connected to a repair via in said second chip site;
29 and

30 electrically connecting said second signal via in said second chip site to
31 that repair via in said second chip site that is connected to said repair via in said first chip
32 site connected to said first signal via.

1 17. A method of repairing an electronic package according to claim 16
2 wherein:

3 (a) the step of isolating said first signal via includes depositing
4 a thin dielectric over said first signal via,

5 (b) the step of isolating said second signal via includes
6 depositing a thin dielectric over said second signal via,

7 (c) the step of electrically connecting said first signal via in
8 said first chip site to that repair via in said first chip site
9 that is connected to a repair via in said second chip site
10 includes depositing a first jumper conductor between said
11 first signal via in said first chip site and that repair via in
12 said first chip site that is connected to a repair via in said
13 second chip site; and

14 (d) the step of electrically connecting said second signal via in
15 said second chip site to that repair via in said second chip
16 site that is connected to said repair via in said first chip site
17 connected to said first signal via includes depositing a
18 second jumper conductor between said second signal via in
19 said second chip site and that repair via in said second chip
20 site that is connected to a repair via in said first chip site.

1 18. A method of repairing an electronic package according to claim 17
2 wherein:

3 (a) the step of electrically connecting said first signal via in
4 said first chip site to that repair via in said first chip site
5 that is connected to a repair via in said second chip site
6 further includes overcoating said first jumper conductor
7 with a dielectric, and

8 (b) the step of electrically connecting said second signal via in
9 said second chip site to that repair via in said second chip
10 site that is connected to said repair via in said first chip site
11 further includes overcoating said second jumper conductor
12 with a dielectric.

1 19. A method of repairing an electronic package according to claim 18:

2 (a) wherein each of said chip sites further includes a ceramic
3 base into which said signal vias and said repair vias extend,
4 and

5 (b) said method further includes the step of firing the electronic
6 package to bond:

7 (1) said thin dielectric over said first signal via to said
8 first signal via,

- 9 (2) said thin dielectric over said second signal via to
10 said second signal via,
- 11 (3) said first jumper conductor to said ceramic base of
12 said chip site having said first signal via and that
13 repair via of the chip site having said first signal via
14 that is connected to that repair via of the chip site
15 having said second signal via,
- 16 (4) said second jumper conductor to said ceramic base
17 of said chip site having said second signal via and
18 that repair via of the chip site having said second
19 signal via that is connected to that repair via of the
20 chip site having said first signal via,
- 21 (5) said dielectric overcoating of said first jumper
22 conductor to said first jumper conductor, and
- 23 (6) said dielectric overcoating of said second jumper
24 conductor to said second jumper conductor.

1 20. A method of repairing an electronic package according to claim 19
2 wherein:

- 3 (a) the step of depositing said first jumper conductor includes
4 depositing said first jumper conductor over said thin
5 dielectric over said first signal via,
- 6 (b) the step of depositing said second jumper conductor
7 includes depositing said second jumper conductor over said
8 thin dielectric over said second signal via,

- 9 (c) the step of overcoating said first jumper conductor with a
10 dielectric includes overcoating said first jumper conductor
11 over said first signal via with said dielectric overcoating
12 said first jumper conductor,
- 13 (d) the step of overcoating said second jumper conductor with
14 a dielectric includes overcoating said second jumper
15 conductor over said second signal via with said dielectric
16 overcoating said second jumper conductor, and
- 17 (e) said method further includes the steps of:
- 18 (1) removing said dielectric overcoating over said first
19 signal via to expose said first jumper conductor over
20 said first signal via, and
- 21 (2) removing said dielectric overcoating over said
22 second signal via to expose said second jumper
23 conductor over said second signal via.